1765

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To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

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Subject: Serial No. 09/867,563 05/31/01

Tsu Shih

A METHOD TO ELIMINATE VIA POISON EFFECT

Grp. Art Unit: 1765

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

U.S. Patent 5,705,430 to Avanzino et al., "Dual Damascene with a Sacrificial Via Fill", describes a dual damascene with a sacrificial fill.

U.S. Patent 6,033,977 to Gutsche et al., "Dual Damascene Structure," describes a method of forming a dual damascene structure using a sacrificial stud in the vial hole.

U.S. Patent 5,422,309 to Zettler et al., "Method for Producing a Metallization Level Having Contacts and Interconnects Connecting the Contacts", describes a method for producing a metallization level having contact and interconnect connecting the contacts.

U.S. Patent 6,051,369 to Azuma et al., "Lithography Process Using One or More Anti-Reflective Coating Films and Fabrication Process Using the Lithography Process", discloses a method of forming a dual damascene using one or more antireflective coating films.

U.S. Patent 5,741,626 to Jain et al., "Method for Forming a Dielectric Tantalum Nitride Layer as an Anti-Reflective Coating (ARC)", discloses the forming of a dual damascene using a particular etch process.

Sincerely,

George O. Saile

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